Toronto Metropolitan University
*Dept. of Electrical, Compute, & Biomedical Eng.*
*ELE 404*

# *Amplifier Design Project*

## Introduction

The purpose of this project is to design, simulate, analyze, implement, and test a single-supply, multistage, inverting, transistor amplifier which fulfills a set of specifications.

For this project, **the pre-lab shall be treated as your formal design report and therefore must be much more detailed than usual** (please see **Evaluation** heading on the next page of this document). **The report shall be submitted to the TA by the deadline.** As with the previous labs, **the report is an individual assignment**.

### Specifications

- Power supply: $+\mathbf{10}\boldsymbol{V}$ relative to the ground;
- Quiescent current drawn from the power supply: ***no larger than*** $\mathbf{10}\ \boldsymbol{mA}$**;**
- No-load voltage gain (at 1 $kHz$): $|\boldsymbol{A_{vo}}| = \mathbf{50}$ $(\pm\ \mathbf{10}\%)$**;**
- Maximum no-load output voltage swing (at 1 $kHz$): ***no smaller than 8 V peak to peak;***
- Loaded voltage gain (at 1 $kHz$ and with $R_L = 1\ k\Omega$): ***no smaller than*** $\mathbf{90}\%$ ***of the no-load voltage gain;***
- Maximum loaded output voltage swing (at 1 $kHz$ and $R_L = 1\ k\Omega$): ***no smaller than 4 V peak to peak;***
- Input resistance (at 1 $kHz$): ***no smaller than*** $\mathbf{20}\ \boldsymbol{k\Omega}$;
- Amplifier type: ***inverting or non-inverting;***
- Frequency response: ***20 Hz to 50 kHz (*** $-\mathbf{3}\boldsymbol{dB}$ ***response);***
- Type of transistors: ***BJT;***
- Number of transistors (stages): ***no more than 3***;
- Resistances permitted: ***values smaller than*** $\mathbf{220}\ \boldsymbol{k\Omega}$ ***from the E24 series***;
- Capacitors permitted: $\mathbf{0.1}\ \boldsymbol{\mu F}$, $\mathbf{1.0}\ \boldsymbol{\mu F}$, $\mathbf{2.2}\ \boldsymbol{\mu F}$, $\mathbf{4.7}\ \boldsymbol{\mu F}$, $\mathbf{10}\ \boldsymbol{\mu F}$, $\mathbf{47}\ \boldsymbol{\mu F}$, $\mathbf{100}\ \boldsymbol{\mu F}$, $\mathbf{220}\ \boldsymbol{\mu F}$**;**
- Other components (BJTs, diodes, Zener diodes, etc.): ***only from your ELE404 lab kit.***

***Notes:***

- The output voltage must be free from distortions (clipping, etc.) in all test conditions.
- The source resistance, $R_s$, must be 600 Ω for all tests.

The designed amplifier must be AC-coupled for the load and the signal source, but the coupling between its intermediate stages may be of AC or DC type as per the designer's choice. There are no restrictions in terms of using NPN or PNP transistors.

Note that there is no right or wrong design, as long as the aforementioned specifications are met.

## Report Content and Length

Including the cover page, the report is limited to 15 pages. In his/her report, the designer must:

1. Identify and justify the types of the constituting amplification stages, which when cascaded will meet the given design requirements (e.g., a CC stage followed by a CE stage, etc., and why…).
2. Present manual calculations for, and explain in sufficient details, his/her selection of the resistance and capacitance values.
3. Simulate the designed amplifier by Multisim (or any other circuit simulation software) and demonstrate that the design indeed meets the requirements and that its simulated performance is in a reasonable agreement with those predicted through manual calculations.

## Evaluation (Read Carefully)

Your report shall be evaluated on the following:

1. Description of the circuit and its choice of configuration (e.g., a CC stage followed by a CE stage, etc., and why…)
2. Manual calculations for the resistance and capacitance values, bias voltages and currents, etc.
3. Detailed simulations of the design, using the circuit elements having come out of the manual calculations of item 2, clearly testing of the amplifier on its adherence to the design specifications (describe each test and provide all the corresponding waveforms).
4. Explanation of discrepancies, if any, between the simulation results and your manual calculation results, and provision of reasons for the discrepancies (to the best of your knowledge).
5. Organization and grammatical structure of the report.

Toronto Metropolitan University

| | |
|---|---|
| **Course Number** | ELE 404 |
| **Course Title** | Electronic Circuits I |
| **Semester/Year** | Winter 2024 |
| **Instructor** | Dr. Fei Yuan |
| **Teacher's Assistant** | Bhagawat Adhikari |

| | |
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| **Lab/Tutorial Report Number** | Project |

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| **Section Number** | 12 |
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| **Student Name** | **Student Number** | **Student Signature** |
|---|---|---|
| Daniel Avella Ordonez | 501212214 | *DA* |
| N/A | N/A | *N/A* |

*By signing above you attest that you have contributed to this submission and confirm that all work you have contributed to this submission is your work. Any suspicion of copying or plagiarism in this work will result in an investigation of Academic Misconduct and may result in a "0" on the work, an "F" in the course, or possibly more severe penalties, as well as a Disciplinary Notice on your academic record under the Student Code of Academic Conduct, which can be found online at:*
*http://www.ryerson.ca/content/dam/senate/policies/pol60.pdf*

## Table of Contents

## Introduction

This report outlines the ELE 404 Amplifier Design Project, an integral part of our electrical engineering curriculum focusing on Bipolar Junction Transistors (BJT). It details the design, simulation, analysis, implementation, and testing phases of a multistage inverting transistor amplifier, adhering to specific constraints such as power supply limits and voltage gain targets. The project blends theoretical knowledge with practical application, demanding creativity and a thorough understanding of electronics. It involves using Multisim for simulation, meticulous pre-lab preparations, and the selection of appropriate transistor configurations. Manual calculations and the rationale behind design choices are documented in the appendix and the body of the report, respectively. This comprehensive exercise evaluates technical skills, problem-solving capabilities, and communication proficiency, marking a critical milestone in our engineering education.

## Objective:

The lab's goal is to design, simulate, analyze, build, and test a single-supply multistage inverting transistor amplifier, following specific criteria. This project aims to enhance practical skills in electronics engineering and deepen understanding of amplifier design by applying theory to meet concrete objectives. It sets forth clear design specifications for the circuit:

- Power supply requirement: +10V relative to ground.
- Quiescent current limit: ≤10mA from the power supply.
- No-load voltage gain at 1kHz: |Avo| = 50 (±10% tolerance).
- Minimum no-load output voltage swing at 1kHz: ≥8V peak-to-peak.
- Loaded voltage gain at 1kHz with a 1kΩ load: ≥90% of no-load gain.
- Minimum loaded output voltage swing at 1kHz with a 1kΩ load: ≥4V peak-to-peak.
- Input resistance at 1kHz: ≥20kΩ.
- Amplifier configuration: either inverting or non-inverting.
- Frequency response range: 20Hz to 50kHz with a -3dB point.
- Transistor requirement: BJT type.
- Transistor stage limit: up to 3 stages.
- Resistance value range: up to 220kΩ, following the E24 series.
- Capacitance options: 0.1µF, 1.0µF, 2.2µF, 4.7µF, 10µF, 47µF, 100µF, 220µF.
- Additional components: restricted to those available in the ELE404 lab kit.

*Notes:*

- Output voltage should remain distortion-free (e.g., no clipping) under all testing scenarios.
- Source resistance, Rs, is set at 600Ω for every test.

**Process for Design and Justifications:**

*Overall Process:*

The ELE 404 Amplifier Design Project combined theoretical learning with practical application, focusing on designing a single-supply multistage inverting transistor amplifier within strict specifications. My approach was systematic, leveraging simulations in Multisim to guide the initial design and refine component selection.

Choosing a common emitter followed by a common collector configuration was key, aimed at balancing amplification with the project's constraints. This decision was informed by analyzing characteristic graphs from Multisim, which helped establish load lines and operating points for the amplifier stages. These graphs were critical for determining component values, particularly for optimizing transistors' transconductance (gm) and base currents.

Simulations played a crucial role throughout, enabling an iterative design process. By adjusting transistor configurations and component values based on simulation feedback, I was able to align the design closely with the project's goals. This iterative approach, grounded in electronic principles, ensured that theoretical insights translated into practical outcomes, guiding the selection of resistors for proper biasing and capacitors for desired frequency response and stability. For a deeper analysis of selected components refer to the manual calculations in the appendix of this lab which outlines the connections between the theoretical approach and its implementation to the practical setting within Multisim.

The final report documents this journey, detailing the rationale behind each design choice, the influence of simulations, and the application of theory to meet the project's specifications. It showcases the challenge of electronic design—balancing theoretical ideals against practical realities—and reflects a comprehensive understanding of amplifier design principles.

*Examination of Graphs:*

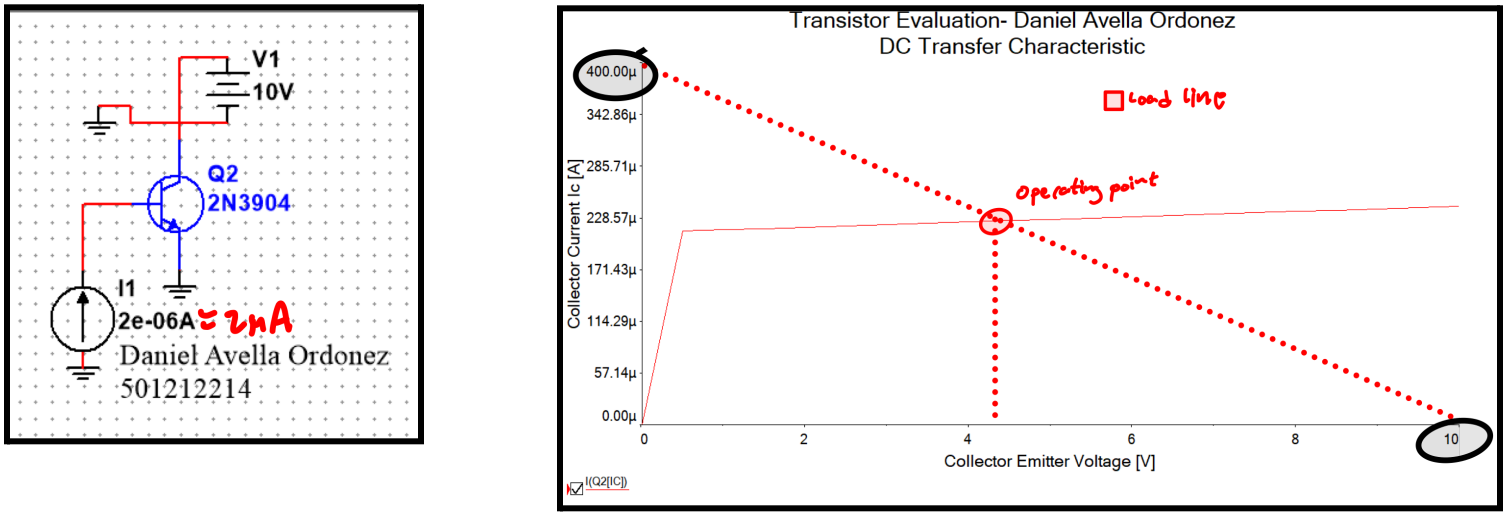


**Figure 1**: Load Line and Operating Point for CE 2N3904 BJT.

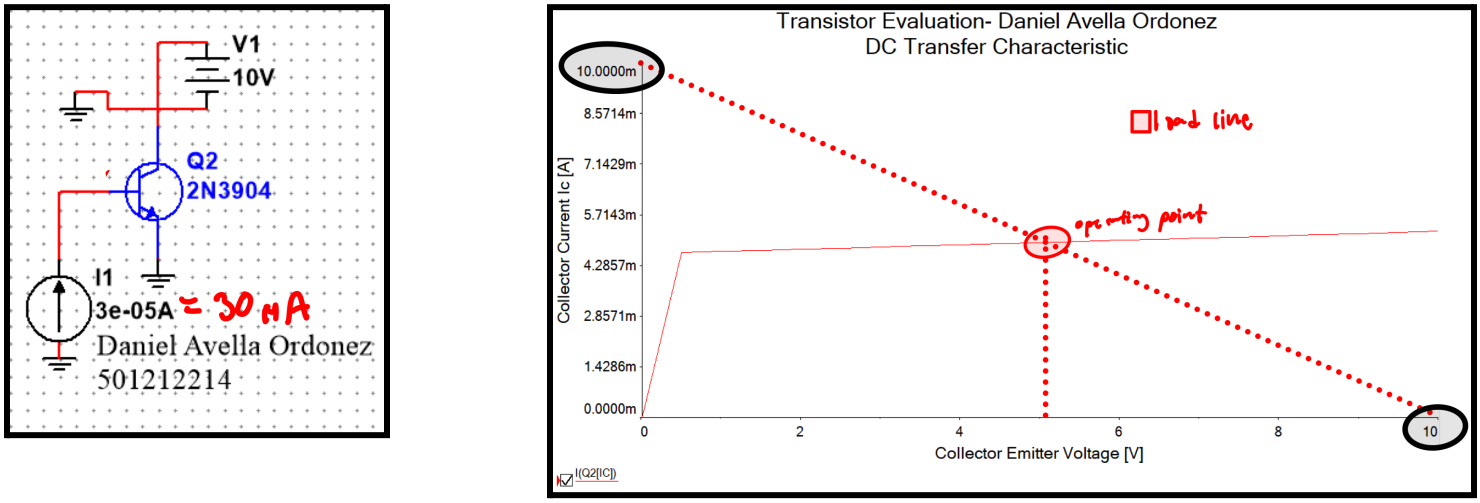


**Figure 2**: Load Line and Operational Characteristics for CC 2N3904 BJT.

Figures 1 and 2, showing the collector current versus the collector-emitter voltage drop for CE and CC 2N3904 BJTs, were crucial in the design process. These graphs helped in two main ways:

1. Identifying Operating Points: By mapping the relationship between collector current and voltage drop, I could draw load lines to find the optimal operating points (Q-points). This was key to ensuring the amplifier worked in its active region, crucial for linear amplification.
2. Calculating Key Parameters: The graphs also allowed for the calculation of important parameters like transconductance (gm) and base currents (IB), ($IB_{DC}$). For instance, the CE stage showed an (IC) of 400 µA at an (IB) of 2 µA, aiding in determining how base current variations influence the collector current.

These insights guided the choice of a CE followed by a CC configuration, leveraging the CE stage for voltage gain and the CC stage for impedance matching, as evidenced by their respective load lines. This analytical approach, underpinned by graph-derived calculations, ensured the design met its goals effectively.

*Resistors:*

The selection of resistors was guided by their critical role in biasing transistors and establishing the desired operating points, directly influencing the amplifier's performance. For example, biasing resistors were chosen to ensure transistors operate within their active regions, crucial for linear amplification. The resistors in the divider network, specifically chosen based on the ELE404 lab kit, such as 91kΩ and 68kΩ, helped maintain stable base voltages, ensuring the circuit met its quiescent current and voltage gain specifications. Adjustments to resistor values, like selecting RC and RE for optimal gain and stability, were made iteratively, based on simulation outcomes and manual calculations, to fine-tune the amplifier's response to meet the project requirements. Please refer to the manual calculations to see in an in-depth analysis of theoretical knowledge.

*Capacitors:*

Capacitor values were crucial for the amplifier's frequency response and stability. We chose 100uF for bypass and 10uF for coupling capacitors to preserve gain across the desired frequency spectrum (20Hz to 50kHz) without losing signal integrity. These choices, aimed at matching the high-input impedance and achieving the right cutoff frequencies, were guided by the formula ($Z=1/(jwC)$). This strategy ensured stable, responsive performance throughout the operational bandwidth and effective signal management between stages. For a detailed theoretical basis, see the manual calculations..

*Summary of Calculations:*

Detailed in the appendix, the manual calculations played a crucial role in meeting the amplifier's specifications for gain, quiescent current, and voltage swing. By optimizing resistor and capacitor values, we ensured proper biasing and stability across the required frequency range. Key outcomes included selecting component values to maximize gain while keeping the quiescent current under 10mA and ensuring consistent amplifier performance from 20Hz to 50kHz. These calculations were vital in aligning the design with project requirements.

**Table 1:** Capacitor Values

| $C_1$ | $C_2$ | $C_3$ | $C_4$ |
|---|---|---|---|
| 10 µF | 100 µF | 10 µF | 100 µF |

**Table 2**: Biasing Resistor Values

| $R_1$ | $R_2$ | $R_3$ | $R_4$ |
|---|---|---|---|
| 91 kΩ | 68 kΩ | 91 kΩ | 200 kΩ |

**Table 3**: Collector and Emitter Resistor Values

| $R_{C1}$ | $R_{E1}$ | $R_{E2}$ | $R_{E3}$ | $R_L$ (Load) |
|---|---|---|---|---|
| 13 kΩ | 15 kΩ | 131 Ω | 10 kΩ | 10 kΩ |

**Table 4:** Critical Values used with respect to the CC (Stage 2)

| $I_B$ | $I_{B,DC}$ | β | $g_m$ | V | $I_C$ |
|---|---|---|---|---|---|
| 65 µA | 30 µA | 153.8 | 0.385 sec | 5 V | 10 mA |

**Table 5:** Critical Values used with respect to the CE (Stage 1)

| $I_B$ | $I_{B,DC}$ | β | $g_m$ | V | $I_C$ |
|---|---|---|---|---|---|
| 3.5 µA | 2 µA | 114.3 | 0.0154 sec | 4.25 V | 400 µA |

**Circuit Under Evaluation:**

The figure below presents the final 2-stage BJT amplifier design, set for simulation in Multisim. This circuit integrates two 2N3904 BJTs (Q1, Q2), nine resistors, and four electrolytic capacitors, powered by a 10V VCC source and stimulated by a sinusoidal signal source (Vs). The equivalent schematic has been carefully constructed in Multisim to facilitate detailed experimental analysis. In the manual calculation section one can view the proposed schematic which ultimately leads to the construction of the proper Multisim circuit below.

**Note:** $R_L$ was adjusted from 1kΩ to 10kΩ to successfully complete the lab requirements and lead to a gain of approximately 50. RE2 was adjusted to 100Ω as this is available in ELE 404 lab kit.

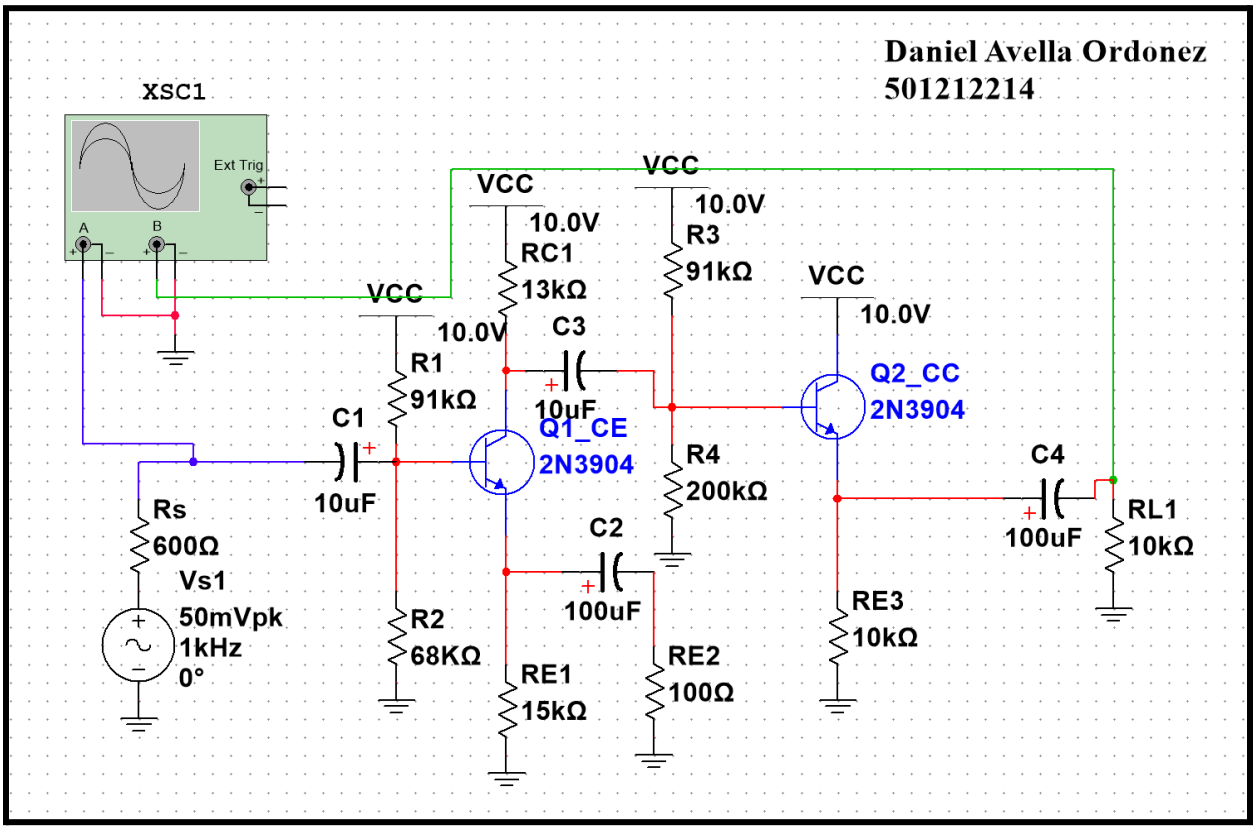


**Figure 3:** Final 2-Stage BJT Amplifier Design for Multisim Simulation

## Experimental Results

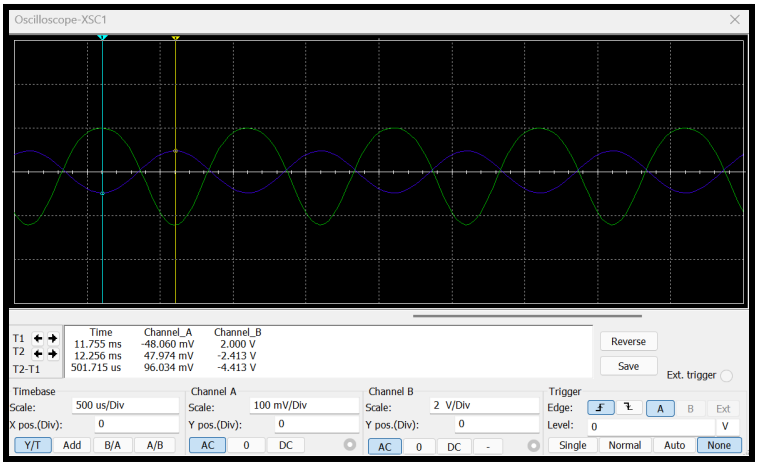


**Figure E1:** The waveform of input voltage and output voltage of Figure 3 ($R_L$= 10 kΩ)

**Table E1:** $V_I$, $V_O$, $A_V$ (loaded voltage gain) with $R_L$= 10 kΩ & *f*=1kHz

| $V_{I\,P\text{-}P}$ [mV] | $V_{O\,P\text{-}P}$ [V] | $A_{VO}$ [V/V] |
|---|---|---|
| 96.034 | 4.413 | 45.952 |

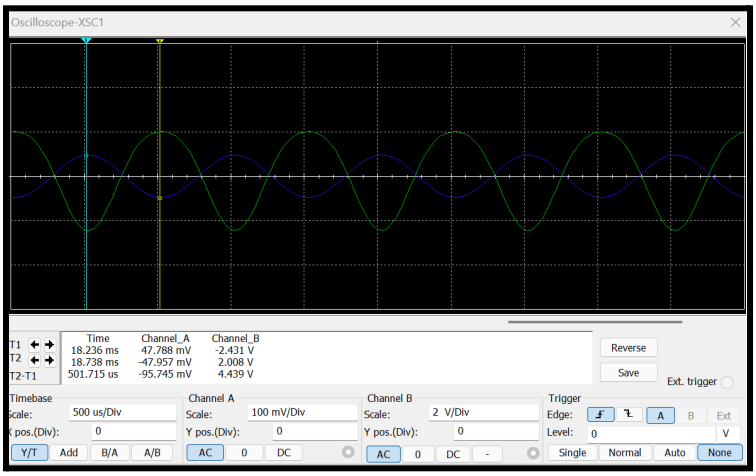


**Figure E2:** The waveform of input voltage and output voltage of Figure 3 ($R_L$=∞)

**Table E2:** $V_I$, $V_O$, $A_V$ (no loaded voltage gain) with $R_L$= ∞ & *f*=1kHz

| $V_{I\,P\text{-}P}$ [mV] | $V_{O\,P\text{-}P}$ [V] | $A_{VO}$ [V/V] |
|---|---|---|
| 95.745 | 4.439 | 46.363 |

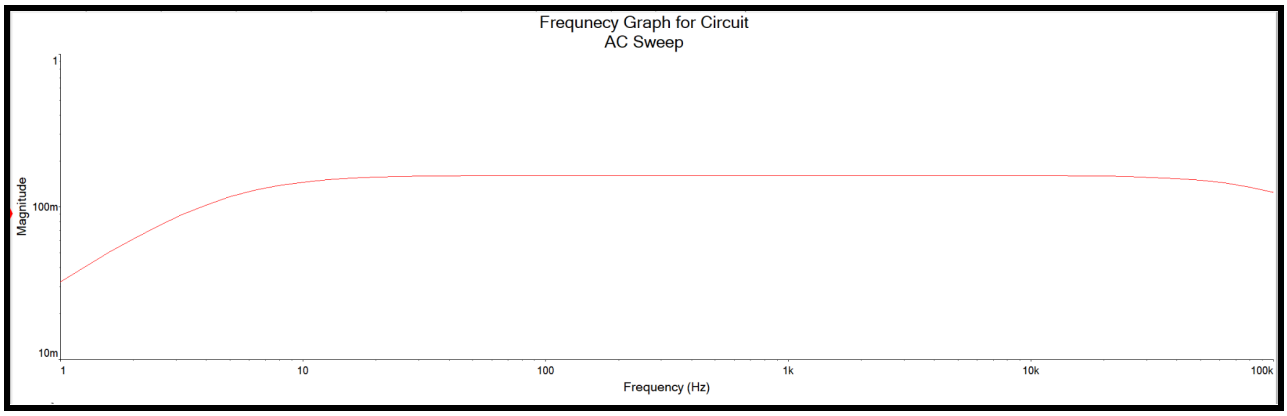


**Figure E3:** The frequency response graph of Figure 3

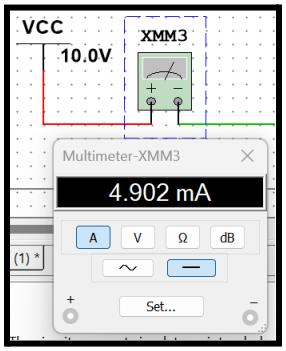


**Figure E4:** The quiescent current drawn from the power supply

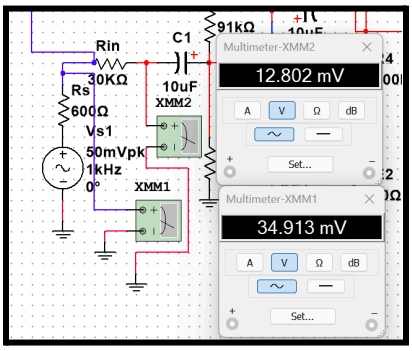


**Figure E5:** The use of Multimeters within the circuit to find input resistance (Ri)

$$R_i = R_{t,in}\left(\frac{v_i}{v_t - v_i}\right)$$

**Table E3:** The parameters used for the equation above to solve for the input resistance ($R_i$)

| $R_i$, Calculated [kΩ] | $R_{test,\ in}$ [kΩ] | $V_t$ [Vrms] | $V_i$ [Vrms] | $R_i$, Experimental [kΩ] |
|---|---|---|---|---|
| 14.497 | 30 | 34.913 mV | 12.802 mV | 17.370 |

**Conclusion**

$$e\% = \frac{calculated\ value - measured\ value}{measured\ value} \times 100$$

**Table C1:** Determining the percent error for the for the design specifications

| Specification | Theoretical Value | Experimental Value | Success (Yes or No) | Percent Error |
|---|---|---|---|---|
| Quiescent current: No larger than 10 mA | 4.94mA | 4.90mA | Yes | 0.82% |
| Avo = 50 (± 10%) | 50.00 | 46.363 | Yes | 7.84% |
| Maximum no-load output voltage swing: No smaller than 8V p-p | 8V | 4.439 | No | 80.29% |
| Loaded voltage gain: No smaller than 90% of Avo | 47.050 | 45.952 (99.113%>90%) | Yes | 2.39% |
| Maximum loaded output voltage swing | 4V | 4.413 $V_{P-P}$ | Yes | 9.36% |
| Input resistance: No smaller than 20 kΩ | 14.497 kΩ | 17.370 kΩ | No | 16.54% |
| Frequency response: 20 Hz to 50 kHz; | *Verified by Figure E3.* | | Yes | N/A |

*Final Remarks*

Upon reviewing Table C1, which outlines the percent errors for our design specifications, it's evident that our 2-stage BJT amplifier, realized through Multisim simulations, largely meets the project's objectives. Notably, we achieved a voltage gain (Avo) of approximately 46.363, closely aligning with the target of 50 within a ±10% tolerance. This outcome underscores the efficacy of our chosen common emitter followed by common collector configuration in attaining the required gain, affirming the design's success in this regard.

However, the project encountered deviations, particularly in achieving the no-load output voltage swing and the input resistance specification. The variance observed in the no-load output voltage swing, deviating significantly from the 8V peak-to-peak expectation, suggests limitations in biasing or the chosen operating points, potentially attributable to the simulation's intrinsic approximations or the load line analysis conducted in Multisim.

The input resistance, targeted to be no smaller than 20kΩ, fell short, with experimental values indicating a lower threshold. This discrepancy may arise from the inherent trade-offs in circuit design, where optimizing for one parameter can impact another. It highlights the complexity of balancing theoretical calculations with practical implementation, especially in a simulated environment where ideal components and conditions are assumed.

In future iterations, addressing these deviations would involve a closer examination of the biasing network and a more nuanced selection of operating points, possibly through iterative simulation refinements or exploring alternative transistor models and configurations. Adjusting the circuit's resistance values and reconsidering the impact of each stage on the overall input impedance could also offer pathways to reconcile these disparities.

Overall, the project's success in meeting its primary objective of achieving a specified gain, alongside the valuable insights gained from the deviations encountered, underscores the learning process's depth. It exemplifies the iterative nature of design, the critical role of simulation in electronic engineering, and the continuous dialogue between theory and practice. This endeavor not only tested our technical acumen but also honed our problem-solving and analytical skills, marking a significant achievement in our educational journey.

References

1. *Design_Project_W2024* (2024). Toronto Metropolitan University - ELE 404 . Retrieved March 30, 2024, from https://courses.torontomu.ca/d2l/le/content/837307/viewContent/5471376/View

**Appendix: Manual Calculations**

*The manual calculations can be viewed in the following pages.*

# MANUAL CALCULATIONS

Design Project Manual Calculations

Daniel Avella Ordonez

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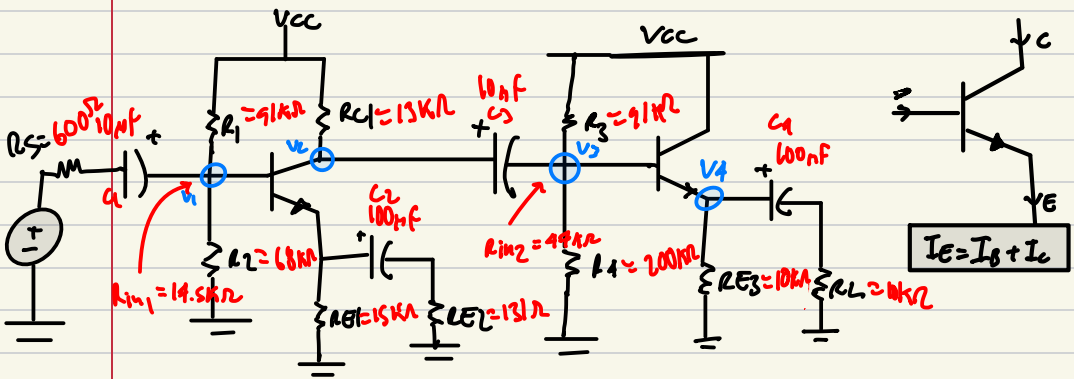



The proposed circuit design: common emitter followed by a common collector configuration.

**Specifications**

- Power supply: $+10V$ relative to the ground;
- Quiescent current drawn from the power supply: ***no larger than*** $\mathbf{10}\ mA$**;**
- No-load voltage gain (at $1\ kHz$): $|A_{vo}| = \mathbf{50}\ (\pm\ \mathbf{10\%})$**;**
- Maximum no-load output voltage swing (at $1\ kHz$): ***no smaller than 8 V peak to peak;***
- Loaded voltage gain (at $1\ kHz$ and with $R_L = 1\ k\Omega$): ***no smaller than*** $90\%$ ***of the no-load voltage gain;***
- Maximum loaded output voltage swing (at $1\ kHz$ and $R_L = 1\ k\Omega$): ***no smaller than 4 V peak to peak;***
- Input resistance (at $1\ kHz$): ***no smaller than*** $\mathbf{20}\ k\Omega$;
- Amplifier type: ***inverting or non-inverting;***
- Frequency response: ***20 Hz to 50 kHz (−3dB response);***
- Type of transistors: ***BJT;***
- Number of transistors (stages): ***no more than 3***;
- Resistances permitted: ***values smaller than*** $\mathbf{220}\ k\Omega$ ***from the E24 series***;
- Capacitors permitted: $\mathbf{0.1}\ \mu F$, $\mathbf{1.0}\ \mu F$, $\mathbf{2.2}\ \mu F$, $\mathbf{4.7}\ \mu F$, $\mathbf{10}\ \mu F$, $\mathbf{47}\ \mu F$, $\mathbf{100}\ \mu F$, $\mathbf{220}\ \mu F$**;**
- Other components (BJTs, diodes, Zener diodes, etc.): ***only from your ELE404 lab kit.***

***Notes:***

- The output voltage must be free from distortions (clipping, etc.) in all test conditions.
- The source resistance, $R_s$, must be 600 Ω for all tests.

Lab Kit Components

| Item | Quantity | Part No. | Description | Check |
|---|---|---|---|---|
| 1 | 2 | 10r | ¼ Watt 5% Resistor | |
| 2 | 5 | 91r | ¼ Watt 5% Resistor | |
| 3 | 2 | 100r | ¼ Watt 5% Resistor | |
| 4 | 2 | 180r | ¼ Watt 5% Resistor | |
| 5 | 2 | 220r | ¼ Watt 5% Resistor | |
| 6 | 2 | 270r | ¼ Watt 5% Resistor | |
| 7 | 2 | 330r | ¼ Watt 5% Resistor | |
| 8 | 2 | 390r | ¼ Watt 5% Resistor | |
| 9 | 2 | 470r | ¼ Watt 5% Resistor | |
| 10 | 2 | 560r | ¼ Watt 5% Resistor | |
| 11 | 2 | 680r | ¼ Watt 5% Resistor | |
| 12 | 2 | 820r | ¼ Watt 5% Resistor | |
| 13 | 2 | 910r | ¼ Watt 5% Resistor | |
| 14 | 5 | 1k0 | ¼ Watt 5% Resistor | |
| 15 | 2 | 1k2 | ¼ Watt 5% Resistor | |
| 16 | 2 | 1k5 | ¼ Watt 5% Resistor | |
| 17 | 2 | 2k2 | ¼ Watt 5% Resistor | |
| 18 | 2 | 2k7 | ¼ Watt 5% Resistor | |
| 19 | 5 | 3k3 | ¼ Watt 5% Resistor | |
| 20 | 2 | 3k9 | ¼ Watt 5% Resistor | |
| 21 | 2 | 4k7 | ¼ Watt 5% Resistor | |
| 22 | 2 | 5k6 | ¼ Watt 5% Resistor | |
| 23 | 2 | 6k8 | ¼ Watt 5% Resistor | |
| 24 | 2 | 9k1 | ¼ Watt 5% Resistor | |
| 25 | 2 | 12k | ¼ Watt 5% Resistor | |
| 26 | 2 | 15k | ¼ Watt 5% Resistor | |
| 27 | 2 | 22k | ¼ Watt 5% Resistor | |
| 28 | 2 | 27k | ¼ Watt 5% Resistor | |
| 29 | 2 | 33k | ¼ Watt 5% Resistor | |
| 30 | 2 | 47k | ¼ Watt 5% Resistor | |
| 31 | 2 | 56k | ¼ Watt 5% Resistor | |
| 32 | 2 | 62k | ¼ Watt 5% Resistor | |
| 33 | 2 | 68k | ¼ Watt 5% Resistor | |
| 34 | 2 | 91k | ¼ Watt 5% Resistor | |
| 35 | 2 | 180k | ¼ Watt 5% Resistor | |
| 36 | 2 | 220k | ¼ Watt 5% Resistor | |
| 37 | 2 | 330k | ¼ Watt 5% Resistor | |
| 38 | 2 | 820k | ¼ Watt 5% Resistor | |
| 39 | 2 | 910k | ¼ Watt 5% Resistor | |
| 40 | 2 | 1M0 | ¼ Watt 5% Resistor | |
| 41 | 2 | 2M2 | ¼ Watt 5% Resistor | |
| 42 | 2 | 10M | ¼ Watt 5% Resistor | |
| 43 | 10 | 10k | ¼ Watt 5% Resistor | |
| 44 | 10 | 100k | ¼ Watt 5% Resistor | |
| 45 | 2 | 0.022uF | Ceramic Capacitor 223 | |
| 46 | 2 | 0.01uF | Ceramic Capacitor 103 | |
| 47 | 6 | 0.1uF | Ceramic Capacitor 104 | |
| 48 | 4 | 1.0uF | Ceramic Capacitor 105 | |
| 49 | 2 | 100uF | 35V Electrolytic Capacitor Radial | |
| 50 | 4 | 10uF | 35V Electrolytic Capacitor Radial | |
| 51 | 4 | 1N4004 | SI-Rectifier Diode | |
| 52 | 10 | 1N4148 | Small Signal Diode | |
| 53 | 2 | 1N4729A | SI-Zener Diode 3.6 Volt | |
| 54 | 2 | 1N4735 | SI-Zener Diode 6.2 Volt | |
| 55 | 2 | 2N3904 | BJT Transistor NPN | |
| 56 | 2 | 2N3906 | BJT Transistor PNP | |
| 57 | 4 | BU-60 | Standard Alligator Clip (Barrel Connection for Banana Plug) | |
| 58 | 1 | Hook up Wire | #22 1 Meter long | |
| 59 | 1 | TL-305 | BNC to Alligator Clip Test Lead | |
| 60 | 1 | Scope Probe | 60MHz Scope Probe 10:1 Circuit Test OP-60A | |
| 61 | 1 | 1k Trim Pot | Mini Trim pot | |
| 62 | 2 | 10k Trim Pot | Mini Trim pot | |
| 63 | 10 | Test Leads | Alligator Clip Test Leads | |
| 64 | 2 | ALD1106PBL | N-Channel MOSFET Transistor Array | |
| 65 | 5 | SSL-LX5093HD | Red LED | |
| 66 | 2 | MCL053GD | Green LED | |

$V_{CC} = 10\ V$

$I_{DC} < 10mA$

$A_{VO} = 50 \pm 10\%$

$V_O \geq 8\ V_{pp}$

$V_L \geq 4\ V_{pp}$

$R_{in} \geq 20\ k\Omega$

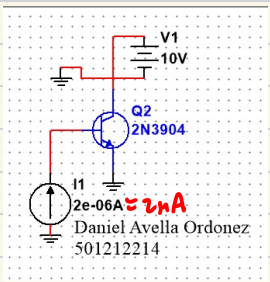
Resistances $\leq 220K\Omega$

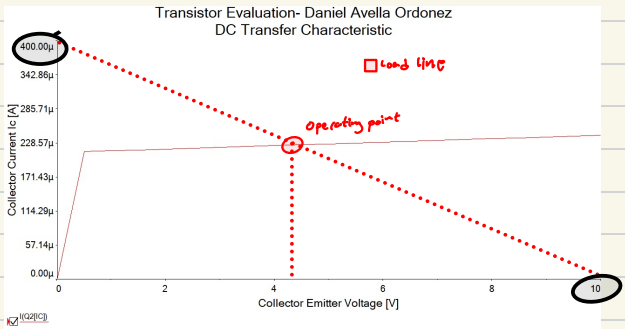
We know that for common collector (CC) the gain is approx. unity which means that AV2= V3/V4=1. We also know from the lab requirements that the total AV gain at the end of our circuit should be 50 V (plus or minus 10%). Thus we have the equation:

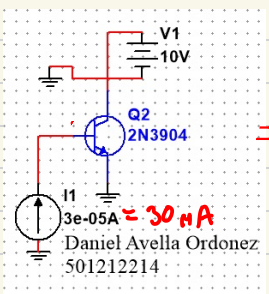
Avo=Avo1*Avo2

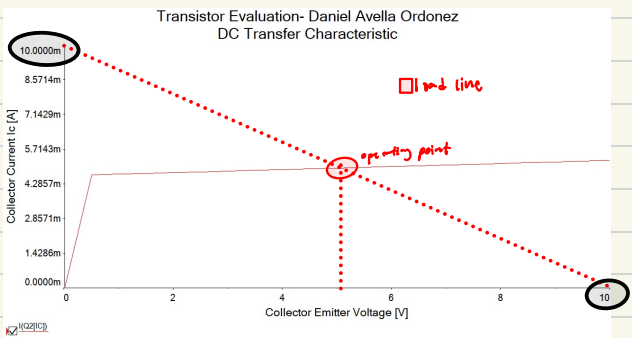
50=Avo1*1

Avo1= 50 (Common Emitter) CE




STAGE 1:

After examining these graphs constructed from Mulitsim we can see that for stage 1 (I.e, CE) that Ic, DC is 400 uA which can be observed from the load line when using 2uA. There for we can calculate the transistors transconductance (gm) for this stage:

gm=Ic/Vt=400uA/26mV=0.0154 seconds

B=400uA/3.5uA=114.3

IB,DC=2 uA (Based on the operating point)

IB,AC=3.5uA

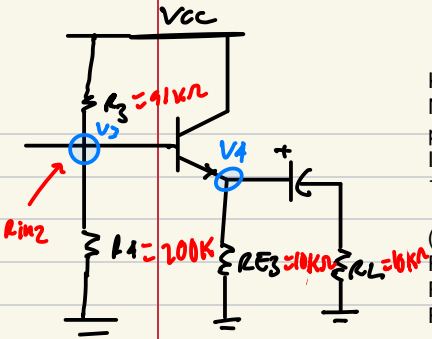
STAGE 2:

Let us assume that RE3=10kohm so that it is close to the RL value. We know from the next graph above that based on the load line Ic=10 mA and IB(DC)=30uA. We also know that IB(AC)=65uA from the load line. We can also calculate the transconductance and B.

gm=10mA/26mV=0.385 seconds

B=Ic/Ib=10mA/65uA=153.8

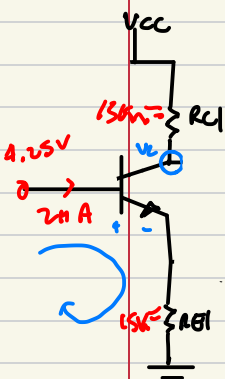
The divider current must be larger than IB to confirm that the voltage at the base is not significantly changed. Hence, 91 kohm is a viable option based on the lab kit for R3




KCL at V3:
Note: We use 5V as an approximation for V3 as can be seen the previous second graph provided. The 30uA is used from the IB,DC graph as well. Also as previously mentioned RE3 is 10kohm due to the loading effect.

(5-10)/(91kohm)+(5)/(R4)+30uA=0
R4=5/24.94 uA
R4=200440.0 ohm
R4=200 Kohm

KVL at node V2:
Note: We can similarly state that the voltage at this examined node is 4.25V based off the first graph previously proposed. Consequently, this means that the entering current at this node is 2uA.




-4.25+0.7+Ie(RE1)=0
RE1=3.55/(1+114.3)(2uA)
RE1=15394.62 ohm
RE1=15 Kohm

Calculations to solve for RC1:
Ic,DC=Vcc/(RC+RE)
RC+RE3=10V/400uA=25 kohm
RC=25-15=10 kohm
RC=10 kohm

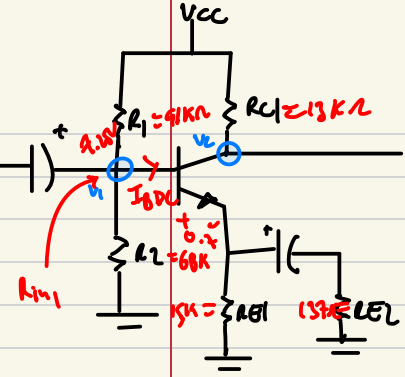
Calculation to solve for Rin2:
Rin2=R3//R4//(B/gm)+(B+1)RE
Rin2=91kohm//200kohm//(153.8/0.385)+154.8(1kohm)
Rin2=44.57 kohm

Calculation to solve for RC1:
1/10kohm=1/RC1+1/44.57kohm
RC1=13 kohm

Now we can solve for RE using the gain equation:
AVO2=V3/V2=((-gm2)(RC1//Rin2)) / (1+gm2*RE)
-50=(-0.0154)(13kohm//44.57kohm) / (1+0.0154*RE)
RE=136.35 ohm
RE=136 ohm

Now we can solve for AV2 (with load). Note that in stage 2 the resistance changed from 1kohm to 500ohm when RL is used as specified in the lab requirements:
Rin2(w/L)= 91kohm//200kohm//(153.8/0.385)+154.8(500ohm)
Rin2(w/L)=34.67 kohm
AVO2(w/L)=(-0.0154)(13kohm//36.67kohm) / (1+0.0154*RE)
AVO2(w/L)=-47.05

Solving for RE2 for stage 1:
RE=136 ohm=RE1//RE2=15kohm//RE2
RE2=137 ohm




Note: Assume that R1 is 91kohm for simple use and since it belongs to the ELE404 lab kit. This ensures that the divider current is greater than the base current by a substantial amount. Note: we assume that the voltage at this node is 4.25 based on the graph 1 we initially proposed

Using KCL to solve for R2:
4.25-10 / 91kohm + 4.25/R2 + 2 uA=0 A
R2=69459.41 ohm
R2= 68 kohm

Solving for Rin1:
Rin1=R1//R2//(B/gm)+(B+1)(RE)
Rin1=91kohm//68kohm//(114.3/0.0154)+(115.3)(136ohm)
Rin1=14 497ohm
Rin1=14.5 kohm

The capacitor values are now determined since the resistor values and all other values are properly calculated. Moreover, the final quiescent current and overall gain will be calculated for the final method to ensure that everything abides by the lab requirements.
Note: The emitter generation resistance is vital to sustain the gain of the common emitter stage. Larger capacitor values are expected for C2 and C4. Since, the Rin1 and Rin2 values are high C1 and C3 do not have to be necessarily as critical/ high value.
We will use the formula:
Z=1/(jwc)
The frequency range is 20Hz-50kHz

$f = 20\ Hz$

$100\ nF\ (C_2, C_4)$: $Z = \frac{1}{j\,2\pi\,(20\,Hz)\,(100\,nF)} = 79.6\,\Omega$

$10\ nF\ (C_1, C_3)$: $Z = \frac{1}{j\,2\pi\,(20\,Hz)\,(10\,nF)} = 796\,\Omega$

$f = 50\,kHz$

$100\ nF\ (C_2, C_4)$: $Z = \frac{1}{j\,2\pi\,(50\,kHz)\,(100\,nF)} = 31.8\,m\Omega$

$10\ nF\ (C_1, C_3)$: $Z = \frac{1}{j\,2\pi\,(50\,kHz)\,(10\,nF)} = 0.32\,\Omega$

$f = 1\,kHz$

$100\ nF\ (C_2, C_4)$: $Z = \frac{1}{j\,2\pi\,(1\,kHz)\,(100\,nF)} = 1.6\,\Omega$

$10\ nF\ (C_1, C_3)$: $Z = \frac{1}{j\,2\pi\,(1\,kHz)\,(10\,nF)} = 15.9\,\Omega$

Therefore, the calculated impedances demonstrate that the capacitors 100uF and 10uF allow the circuit to maintain its gain
Final Circuit Gain:
Avo=1*50=50.00
Av= 1*47.05=47.05
We multiply by 1 since stage 2 is a common collector which means that at this stage there is unity (multi-tile of 1) with stage 1 being the common collector which was have calculated to have a gain of approximately 50.
Quiescent current:
I(DC) total= IC1+IR1+IC2+IR3
I(DC) total= B(IB1)+ VCC/(R1+R2) + BIB2 + VCC/(R3+R4)
I(DC) total=114.3(2uA) + 10/(91kohm+68kohm) + 153.8(30uA) + 10/(200kohm+91kohm)
I(DC) total= 0.00494A = 4.94 mA
4.94mA<10mA which satisfies the lab requirement
Therefore, all lab requirements are satisfied and the manual calculations for this lab project was successfull.